CLAIMS

1. A free-standing and bulk-doped semiconductor comprising at least one portion having a smallest width of less than 500 nanometers.

2. The semiconductor of claim 1, wherein the semiconductor comprises:

an interior core comprising a first semiconductor; and

one or more exterior shells exterior to the interior core, at least one of the exterior shells comprising a different material than the first semiconductor.

3. The semiconductor of claim 1, wherein the semiconductor comprises an elemental semiconductor.

4. The semiconductor of claim 3, wherein the elemental semiconductor is selected from a group consisting of: Si, Ge, Sn, Se, Te, B, Diamond and P.

5. The semiconductor of claim 1, wherein the semiconductor comprises a solid solution of elemental semiconductors.

6. The semiconductor of claim 5, wherein the solid solution is selected from a group consisting of: B-C, B-P(BP6), B-Si, Si-C, Si-Ge, Si-Sn and Ge-Sn.

7. The semiconductor of claim 1, wherein the semiconductor comprises a Group IV-Group IV semiconductor.

8. The semiconductor of claim 7, wherein the Group IV-Group IV semiconductor is SiC.

9. The semiconductor of claim 1, wherein the semiconductor comprises a Group III-Group V semiconductor.

10. The semiconductor of claim 9, wherein the Group III-Group V semiconductor is selected from a group consisting of: BN/BP/BAs, AlN/AlP/AlAs/AlSb,

GaN/GaP/GaAs/GaSb, InN/InP/InAs/InSb.

11. The semiconductor of claim 1, wherein the semiconductor comprises an alloy comprising a combination of two or more Group III-Group V semiconductors from a group consisting of: BN/BP/BAs, AlN/AlP/AlAs/AlSb, GaN/GaP/GaAs/GaSb, InN/InP/InAs/InSb.

12. The semiconductor of claim 1, wherein the semiconductor comprises a Group II-Group VI semiconductor.

13. The semiconductor of claim 12, wherein the semiconductor is selected from a group consisting of: ZnO/ZnS/ZnSe/ZnTe, CdS/CdSe/CdTe, HgS/HgSe/HgTe, BeS/BeSe/BeTe/MgS/MgSe.

14. The semiconductor of claim 1, wherein the semiconductor comprises an alloy comprising a combination of two or more Group II-Group VI semiconductors from a group consisting of: ZnO/ZnS/ZnSe/ZnTe, CdS/CdSe/CdTe, HgS/HgSe/HgTe, BeS/BeSe/BeTe/MgS/MgSe.

15. The semiconductor of claim 1, wherein the semiconductor comprises an alloy comprising a combination of a Group II-Group VI semiconductors from a group consisting of: ZnO/ZnS/ZnSe/ZnTe, CdS/CdSe/CdTe, HgS/HgSe/HgTe, BeS/BeSe/BeTe/MgS/MgSe and a Group III-Group V semiconductors from a group consisting of: BN/BP/BAs, AlN/AlP/AlAs/AlSb, GaN/GaP/GaAs/GaSb, InN/InP/InAs/InSb.

16. The semiconductor of claim 1, wherein the semiconductor comprises a Group IV-Group VI semiconductor.

17. The semiconductor of claim 16, wherein the semiconductor is selected from a group consisting of: GeS, GeSe, GeTe, SnS, SnSe, SnTe, PbO, PbS, PbSe, PbTe

18. The semiconductor of claim 1, wherein the semiconductor comprises a Group I-Group VII semiconductor.

19. The semiconductor of claim 18, wherein the semiconductor is selected from a group consisting of: CuF, CuCl, CuBr, CuI, AgF, AgCl, AgBr, AgI.

20. The semiconductor of claim 1, wherein the semiconductor comprises a semiconductor selected from a group consisting of: BeSiN2, CaCN2, ZnGeP2, CdSnAs2, ZnSnSb2, CuGeP3, CuSi2P3, (Cu, Ag)(Al, Ga, In, Tl, Fe)(S, Se, Te)2, Si3N4, Ge3N4, Al2O3, (Al, Ga, In)2(S, Se, Te)3 and Al2CO.

21. The semiconductor of claim 1, wherein the semiconductor comprises a p-type dopant.

22. The semiconductor of claim 1, wherein the semiconductor comprises an n-type dopant from.

23. The semiconductor of claim 1, wherein the semiconductor comprises a p-type dopant from Group III of the periodic table.

24. The semiconductor of claim 1, wherein the semiconductor comprises an n-type dopant from Group V of the periodic table.

25. The semiconductor of claim 1, wherein the semiconductor comprises a p-type dopant selected from a group consisting of: B, Al and In.

26. The semiconductor of claim 1, wherein the semiconductor comprises an n-type dopant selected from a group consisting of: P, As and Sb.

27. The semiconductor of claim 1, wherein the semiconductor comprises a p-type dopant from Group II of the periodic table.

28. The semiconductor of claim 27, wherein the p-type dopant is selected from a group consisting of: Mg, Zn, Cd and Hg.

29. The semiconductor of claim 1, wherein the semiconductor comprises a p-type dopant from Group IV of the periodic table.

30. The semiconductor of claim 29, wherein the p-type dopant is selected from a group consisting of: C and Si.

31. The semiconductor of claim 27, wherein the n-type is selected from a group consisting of: Si, Ge, Sn, S, Se and Te.

32. The semiconductor of claim 1, wherein the smallest width is less than 200 nanometers.

33. The semiconductor of claim 1, wherein the smallest width is less than 150 nanometers.

34. The semiconductor of claim 1, wherein the smallest width is less than 100 nanometers.

35. The semiconductor of claim 1, wherein the smallest width is less than 80 nanometers.

36. The semiconductor of claim 1, wherein the smallest width is less than 70 nanometers.

37. The semiconductor of claim 1, wherein the smallest width is less than 60 nanometers.

38. The semiconductor of claim 1, wherein the smallest width is less than 40 nanometers.

39. The semiconductor of claim 1, wherein the smallest width is less than 20 nanometers.

40. The semiconductor of claim 1, wherein the smallest width is less than 10 nanometers

41. The semiconductor of claim 1, wherein the smallest width is less than 5 nanometers

42. The semiconductor of claim 1, wherein the semiconductor is elongated, and the at least one portion is a longitudinal section.

43. The semiconductor of claim 42, wherein the longitudinal section, a ratio of the length of the section to a longest width is greater than 4:1.

44. The semiconductor of claim 42, wherein the longitudinal section, a ratio of the length of the section to a longest width is greater than 10:1.

45. The semiconductor of claim 42, wherein the longitudinal section, a ratio of the length of the section to a longest width is greater than 100:1.

46. The semiconductor of claim 42, wherein the longitudinal section, a ratio of the length of the section to a longest width is greater than 1000:1.

47. The semiconductor of claim 1, wherein the semiconductor comprises a single crystal.

48. The semiconductor of claim 1, wherein the semiconductor is part of a device.

49. The semiconductor of claim 1, wherein the semiconductor is n-doped.

50. The semiconductor of claim 1, wherein the semiconductor is p-doped.

51. The semiconductor of claim 1, wherein the semiconductor is magnetic.

52. The semiconductor of claim 51, wherein the semiconductor comprises a dopant making the semiconductor magnetic.

53. The semiconductor of claim 51, wherein the semiconductor is ferromagnetic.

54. The semiconductor of claim 53, wherein the semiconductor comprises a dopant that makes the semiconductor ferromagnetic.

55. The semiconductor of claim 54, wherein the semiconductor comprises manganese.

56. An elongated and bulk-doped semiconductor that, at any point along its longitudinal axis, has a largest cross-sectional dimension less than 500 nanometers.

57. The semiconductor of claim 56, wherein the semiconductor comprises:

an interior core comprising a first semiconductor; and

one or more exterior shells exterior to the interior core, at least one of the exterior shells comprising a different material than the first semiconductor.

58. The semiconductor of claim 56, wherein, at any point along the longitudinal axis of the semiconductor, a ratio of the length of the section to a longest width is greater than 4:1.

59. The semiconductor of claim 56, wherein, at any point along the longitudinal axis of the semiconductor, a ratio of the length of the section to a longest width is greater than 10:1.

60. The semiconductor of claim 56, wherein, at any point along the longitudinal axis of the semiconductor, a ratio of the length of the section to a longest width is greater than 100:1

61. The semiconductor of claim 56, wherein, at any point along the longitudinal axis of the semiconductor, a ratio of the length of the section to a longest width is greater than 1000:1

62. The semiconductor of claim 56, wherein the point has a smallest width less than 200 nanometers.

63. The semiconductor of claim 56, wherein the point has a smallest width less than 150 nanometers.

64. The semiconductor of claim 56, wherein the point has a smallest width less than 100 nanometers.

65. The semiconductor of claim 56, wherein the point has a smallest width less than 80 nanometers.

66. The semiconductor of claim 56, wherein the point has a smallest width less than 70 nanometers.

67. The semiconductor of claim 56, wherein the point has a smallest width less than 60 nanometers.

68. The semiconductor of claim 56, wherein the point has a smallest width less than 40 nanometers.

69. The semiconductor of claim 56, wherein the point has a smallest width less than 20 nanometers.

70. The semiconductor of claim 56, wherein the point has a smallest width less than 10 nanometers.

71. The semiconductor of claim 56, wherein the point has a smallest width less than 5 nanometers.

72. The semiconductor of claim 56, wherein the semiconductor comprises a single crystal.

73. The semiconductor of claim 56, wherein the semiconductor is free-standing.

74. The semiconductor of claim 56, wherein the semiconductor is part of a device.

75. The semiconductor of claim 56, wherein the semiconductor is n-doped.

76. The semiconductor of claim 56, wherein the semiconductor is p-doped.

77. A doped semiconductor comprising a single crystal.

78. The semiconductor of claim 77, wherein the semiconductor comprises:
an interior core comprising a first semiconductor; and
one or more exterior shells exterior to the interior core, at least one of the exterior shells comprising a different material than the first semiconductor.

79. The semiconductor of claim 77, wherein the semiconductor is bulk-doped.

80. The semiconductor of claim 77, wherein the semiconductor is free-standing.

81. The semiconductor of claim 77, wherein the semiconductor comprises a portion having a width of less than 500 nanometers.

82. The semiconductor of claim 77, wherein the semiconductor is elongated.

83. The semiconductor of claim 77, wherein the semiconductor is part of a device.

84. The semiconductor of claim 77, wherein the semiconductor is n-doped.

85. The semiconductor of claim 77, wherein the semiconductor is p-doped.

86. A doped semiconductor that was doped during growth of the semiconductor.

87. The semiconductor of claim 86, wherein the doped semiconductor was grown by applying energy to one or more molecules of the semiconductor and one or more molecules of a dopant.

88. The semiconductor of claim 86, wherein the doped semiconductor was grown by applying energy to one or more molecules of the semiconductor and one or more molecules of a dopant.

89. The semiconductor of claim 86, wherein the doped semiconductor was grown by applying energy to one or more molecules of the semiconductor and one or more molecules of a dopant.

90. The semiconductor of claim 86, wherein the semiconductor is bulk-doped.

91. The semiconductor of claim 86, wherein the semiconductor comprises a single crystal.

92. The semiconductor of claim 86, wherein the semiconductor is free-standing.

93. The semiconductor of claim 86, wherein the semiconductor comprises a portion having a width of less than 500 nanometers.

94. The semiconductor of claim 86, wherein the semiconductor is elongated.

95. The semiconductor of claim 86, wherein the semiconductor is n-doped.

96. The semiconductor of claim 86, wherein the semiconductor is p-doped.

97. A bulk-doped semiconductor that is at least one of the following: a single crystal, an elongated and bulk-doped semiconductor that, at any point along its longitudinal axis, has a largest cross-sectional dimension less than 500 nanometers, and a free-standing and bulk-doped semiconductor with at least one portion having a smallest width of less than 500 nanometers, wherein a phenomena produced by a section of the bulk-doped semiconductor exhibits a quantum confinement caused by a dimension of the section.

98. The semiconductor of claim 97, wherein the semiconductor is elongated and the dimension is a width at any point along a longitudinal section of the semiconductor.

99. The semiconductor of claim 98, wherein the longitudinal section is capable of transporting electrical carriers without scattering.

100. The semiconductor of claim 99, wherein the longitudinal section is capable of transporting electrical carriers such that the electrical carriers pass through the longitudinal section ballistically.

101. The semiconductor of claim 99, wherein the longitudinal section is capable of transporting electrical carriers such that the electrical carriers pass through the longitudinal section coherently.

102. The semiconductor of claim 98, wherein the longitudinal section is capable of transporting electrical carriers such that the electrical carriers are spin-polarized.

103. The semiconductor of claim 102, wherein the longitudinal section is capable of transporting electrical carriers such that the spin-polarized electrical carriers pass through the longitudinal section without losing spin information.

104. The semiconductor of claim 98, wherein the longitudinal section is capable of emitting light in response to excitation, wherein a wavelength of the emitted light is

related to the width.

105. The semiconductor of claim 99, wherein the wavelength of the emitted light is proportional to the width.

106. A bulk-doped semiconductor that exhibits coherent transport.

107. A bulk-doped semiconductor that exhibits ballistic transport.

108. A bulk-doped semiconductor that exhibits Luttinger liquid behavior.

109. A solution comprising one or more doped semiconductors, wherein at least one of the semiconductors is at least one of the following: a single crystal, an elongated and bulk-doped semiconductor that, at any point along its longitudinal axis, has a largest cross-sectional dimension less than 500 nanometers, and a free-standing and bulk-doped semiconductor with at least one portion having a smallest width of less than 500 nanometers.

110. A device comprising at least one doped semiconductor, wherein the at least one doped semiconductor is at least one of the following: a single crystal, an elongated and bulk-doped semiconductor that, at any point along its longitudinal axis, has a largest cross-sectional dimension less than 500 nanometers, and a free-standing and bulk-doped semiconductor with at least one portion having a smallest width of less than 500 nanometers.

111. The device of claim 110, wherein the device comprises at least two doped semiconductors, wherein both of the at least two doped semiconductors is at least one of the following: a single crystal, an elongated and bulk-doped semiconductor that, at any point along its longitudinal axis, has a largest cross-sectional dimension less than 500 nanometers, and a free-standing and bulk-doped semiconductor with at least one portion having a smallest width of less than 500 nanometers, and wherein a first of the at least two doped semiconductors exhibits quantum confinement and a second of the at least two

doped semiconductor manipulates the quantum confinement of the first.

112. The device of claim 110, wherein the device comprises at least two doped semiconductor, wherein both of the at least two doped semiconductors is at least one of the following: a single crystal, an elongated and bulk-doped semiconductor that, at any point along its longitudinal axis, has a largest cross-sectional dimension less than 500 nanometers, and a free-standing and bulk-doped semiconductor with at least one portion having a smallest width of less than 500 nanometers.

113. The device of claim 111, wherein the at least two bulk-doped semiconductors are in physical contact with each other.

114. The device of claim 113, wherein a first of the at least two bulk-doped semiconductors is of a first conductivity type, and a second of the at least two bulk-doped semiconductors is of a second conductivity type.

115. The device of claim 114, wherein the first conductivity type is n-type, and the second type of conductivity type is p-type.

116. The device of claim 115, wherein the at least two bulk-doped semiconductors form a p-n junction.

117. The device of claim 110, wherein the at least one semiconductor is free-standing.

118. The device of claim 110, wherein the at least one semiconductor is elongated.

119. The device of claim 110, wherein the at least one semiconductor comprises a single crystal.

120. The device of claim 110, wherein the at least one semiconductor comprises:
an interior core comprising a first semiconductor; and
an exterior shell comprising a different material than the first semiconductor.

121. The device of claim 110, wherein the device comprises a switch.

122. The device of claim 110, wherein the device comprises a diode.

123. The device of claim 110, wherein the device comprises a Light-Emitting Diode.

124. The device of claim 110, wherein the device comprises a tunnel diode.

125. The device of claim 110, wherein the device comprises a Schottky diode.

126. The device of claim 125, wherein the transistor comprises a Bipolar Junction Transistor.

127. The device of claim 125, wherein the transistor comprises a Field Effect Transistor.

128. The device of claim 110, wherein the device comprises an inverter.

129. The device of claim 128, wherein the inverter is a complimentary inverter.

130. The device of claim 110, wherein the device comprises an optical sensor.

131. The device of claim 110, wherein the device comprises a sensor for an analyte.

132. The device of claim 110, wherein the analyte is a DNA.

133. The device of claim 110, wherein the device comprises a memory device.

134. The device of claim 133, wherein the memory device is a dynamic memory device.

135. The device of claim 133, wherein the memory device is a static memory device.

136. The device of claim 110, wherein the device comprises a laser.

137. The device of claim 110, wherein the device comprises a logic gate.

138. The device of claim 137, wherein the logic gate is an AND gate.

139. The device of claim 137, wherein the logic gate is a NAND gate.

140. The device of claim 137, wherein the logic gate is an EXCLUSIVE-AND gate.

141. The device of claim 137, wherein the logic gate is a OR gate.

142. The device of claim 137, wherein the logic gate is a NOR gate.

143. The device of claim 137, wherein the logic gate is an EXCLUSIVE-OR gate.

144. The device of claim 110, wherein the device comprises a latch.

145. The device of claim 110, wherein the device comprises a register.

146. The device of claim 110, wherein the device comprises clock circuitry.

147. The device of claim 110, wherein the device comprises a logic array.

148. The device of claim 110, wherein the device comprises a state machine.

149. The device of claim 110, wherein the device comprises a programmable circuit.

150. The device of claim 110, wherein the device comprises an amplifier.

151. The device of claim 110, wherein the device comprises a transformer.

152. The device of claim 110, wherein the device comprises a signal processor.

153. The device of claim 110, wherein the device comprises a digital circuit.

154. The device of claim 110, wherein the device comprises an analog circuit.

155. The device of claim 110, wherein the device comprises a light emission source.

156. The device of claim 155, wherein the light emission source emits light at a higher frequency than would the semiconductor if the semiconductor had a shortest width greater than the shortest width at any portion of the semiconductor.

157. The device of claim 110, wherein the device comprises a photoluminescent device.

158. The device of claim 110, wherein the device comprises an electroluminescent device.

159. The device of claim 110, wherein the device comprises a rectifier.

160. The device of claim 110, wherein the device comprises a photodiode.

161. The device of claim 110, wherein the device comprises a p-n solar cell.

162. The device of claim 110, wherein the device comprises a phototransistor.

163. The device of claim 110, wherein the device comprises a single-electron transistor.

164. The device of claim 110, wherein the device comprises a single photon emitter.

165. The device of claim 110, wherein the device comprises a single photon detector.

166. The device of claim 110, wherein the device comprises a spintronic device.

167. The device of claim 110, wherein the device comprises an ultra-sharp tip for atomic force microscope.

168. The device of claim 110, wherein the device comprises a scanning tunneling microscope.

169. The device of claim, wherein the device comprises a field emission device

170. The device of claim, wherein the device comprises a photoluminescence tag

171. The device of claim, wherein the device comprises a photovoltaic device

172. The device of claim, wherein the device comprises photonic band gap materials

173. The device of claim 110, wherein the device comprises a scanning near field optical microscope tips.

174. The device of claim 110, wherein the device comprises a circuit that has digital and analog components.

175. The device of claim 110, wherein the device comprises another semiconductor that is electrically coupled to the at least one bulk-doped semiconductor.

176. The device of claim 175, wherein the other semiconductor is a bulk-doped semiconductor comprising at least one portion having a smallest width of less than 500 nanometers.

177. The device of claim 110, wherein the device comprises another semiconductor that is optically coupled to the at least one bulk-doped semiconductor.

178. The device of claim 177, wherein the other semiconductor is a bulk-doped semiconductor comprising at least one portion having a smallest width of less than 500

nanometers.

179. The device of claim 110, wherein the device comprises another semiconductor that is magnetically coupled to the at least one bulk-doped semiconductor.

180. The device of claim 179, wherein the other semiconductor is a bulk-doped semiconductor comprising at least one portion having a smallest width of less than 500 nanometers.

181. The device of claim 110, wherein the device comprises another semiconductor that physically contacts the at least one bulk-doped semiconductor.

182. The device of claim 179, wherein the other semiconductor is at least one of the following: a single crystal, an elongated and bulk-doped semiconductor that, at any point along its longitudinal axis, has a largest cross-sectional dimension less than 500 nanometers, and a free-standing and bulk-doped semiconductor with at least one portion having a smallest width of less than 500 nanometers.

183. The device of claim 110, wherein the at least one semiconductor is coupled to an electrical contact.

184. The device of claim 110, wherein the at least one semiconductor is coupled to an optical contact.

185. The device of claim 110, wherein the at least one semiconductor is coupled to a magnetic contact.

186. The device of claim 110, wherein a conductivity of the at least one semiconductor is controllable in response to a signal.

187. The device of claim 186, wherein the conductivity of the at least one semiconductor is controllable to have any value within a range of values.

188. The device of claim 186, wherein the at least one semiconductor is switchable between two or more states.

189. The device of claim 188, wherein the at least one semiconductor is switchable between a conducting state and an insulating state by the signal.

190. The device of claim 188, wherein two or more states of the at least one semiconductor are maintainable without an applied signal.

191. The device of claim 186, wherein the conductivity of the at least one semiconductor is controllable in response to an electrical signal.

192. The device of claim 186, wherein the conductivity of the at least one semiconductor is controllable in response to an optical signal.

193. The device of claim 186, wherein the conductivity of the at least one semiconductor is controllable in response to a magnetic signal.

194. A device of claim 186, wherein the conductivity of the at least one semiconductor is controllable in response to a signal of a gate terminal.

195. The device of claim 194, wherein the gate terminal is not in physical contact with the at least one semiconductor.

196. The device of claim 110, wherein at least two of the semiconductors form an array, and at least one of the semiconductors in the array is at least one of the following: a single crystal, an elongated and bulk-doped semiconductor that, at any point along its longitudinal axis, has a largest cross-sectional dimension less than 500 nanometers, and a free-standing and bulk-doped semiconductor with at least one portion having a smallest width of less than 500 nanometers.

197. The device of claim 196, wherein the array is an ordered array.

198. The device of claim 196, wherein said array is not an ordered array.

199. The device of claim 110, wherein the device comprises two or more separate and interconnected circuits, at least one of the circuits not comprising a doped semiconductor that is at least one of the following: a single crystal, an elongated and bulk-doped semiconductor that, at any point along its longitudinal axis, has a largest cross-sectional dimension less than 500 nanometers, and a free-standing and bulk-doped semiconductor with at least one portion having a smallest width of less than 500 nanometers.

200. The device of claim 110, wherein the device is embodied on a chip having one or more pinouts

201. The device of claim 200, wherein the chip comprises separate and interconnected circuits, at least one of the circuits not comprising a doped semiconductor that is at least one of the following: a single crystal, an elongated and bulk-doped semiconductor that, at any point along its longitudinal axis, has a largest cross-sectional dimension less than 500 nanometers, and a free-standing and bulk-doped semiconductor with at least one portion having a smallest width of less than 500 nanometers.

202. A collection of reagents for growing a doped semiconductor that will be at least one of the following: a single crystal, an elongated and bulk-doped semiconductor that, at any point along its longitudinal axis, has a largest cross-sectional dimension less than 500 nanometers, and a free-standing and bulk-doped semiconductor with at least one portion having a smallest width of less than 500 nanometers that comprises at least one portion having a smallest width of less than 500 nanometers,

wherein the collection comprises a semiconductor reagent and a dopant reagent.

203. A method of growing a semiconductor, the method comprising an act of:

(A) doping the semiconductor during growth of the semiconductor.

204. The method of claim 203, wherein the grown semiconductor is a doped semiconductor that is at least one of the following: a single crystal, an elongated and bulk-doped semiconductor that, at any point along its longitudinal axis, has a largest cross-

sectional dimension less than 500 nanometers, and a free-standing and bulk-doped semiconductor with at least one portion having a smallest width of less than 500 nanometers.

205. The method of claim 203, further comprising an act of:

(B) adding one or more other materials to a surface of the doped semiconductor.

206. The method of claim 205, wherein act (B) comprises forming a shell around the doped semiconductor.

207. The method of claim 203, wherein act (A) comprises:

controlling an extent of the doping.

208. The method of claim 203, wherein act (A) comprises growing the doped semiconductor by applying energy to a collection of molecules, the collection of molecules comprising molecules of the semiconductor and molecules of a dopant.

209. The method of claim 208, wherein act (A) comprises an act of:

controlling an extent of the doping.

210. The method of claim 209, wherein the act of controlling doping comprises controlling a ratio of an amount of the semiconductor molecules to an amount of the dopant molecules.

211. The method of claim 209, wherein act (A) further comprises:

vaporizing the molecules using a laser to form vaporized molecules.

212. The method of claim 211, wherein act (A) further comprises:

growing the semiconductor from the vaporized molecules.

213. The method of claim 211, wherein act (A) further comprises:
condensing the vaporized molecules into a liquid cluster.

214. The method of claim 212, wherein act (A) further comprises:
growing the semiconductor from the liquid cluster.

215. The method of claim 211, wherein act (A) is performed using laser-assisted catalytic growth.

216. The method of claim 208, wherein the collection of molecules comprises a cluster of molecules of a catalyst material.

217. The method of claim 216, wherein act (A) comprises:
controlling a width of the semiconductor.

218. The method of claim 217, wherein controlling the width of the semiconductor comprises:
controlling a width of the catalyst cluster.

219. The method of claim 203, wherein act (A) further comprises:
performing chemical vapor deposition on at least the molecules.

220. The method of claim 203, wherein the grown semiconductor has at least one portion having a smallest width of less than 20 nanometers.

221. The method of claim 220, wherein the grown semiconductor has at least one portion having a smallest width of less than 10 nanometers.

222. The method of claim 220, wherein the grown semiconductor has at least one portion having a smallest width of less than 5 nanometers.

223. The method of claim 203, wherein the grown semiconductor is magnetic.

224. The method of claim 223, wherein act (A) comprises:

doping the semiconductor with a material that makes the grown semiconductor magnetic.

225. The method of claim 203, wherein the grown semiconductor is ferromagnetic.

226. The method of claim 225, act (A) comprises:

doping the semiconductor with a material that makes the grown semiconductor ferromagnetic.

227. The method of claim 226, wherein act (A) comprises:

doping the semiconductor with manganese.

228. A method of fabricating a device, comprising an act of:

(A) contacting one or more semiconductors to a surface, wherein at least one of the semiconductors is at least one of the following: a single crystal, an elongated and bulk-doped semiconductor that, at any point along its longitudinal axis, has a largest cross-sectional dimension less than 500 nanometers, and a free-standing and bulk-doped semiconductor with at least one portion having a smallest width of less than 500 nanometers.

229. The method of claim 228, wherein the surface is a substrate.

230. The method of claim 228, further comprising an act of:

(B) prior to act (A), growing at least one of the semiconductors by applying energy to molecules of a semiconductor and molecules of a dopant.

231. The method of claim 228, wherein act (A) comprises:

contacting a solution comprising the one or more semiconductors to the surface.

232. The method of claim 231, further comprising:

(B) aligning one or more of the semiconductors on the surface using an electric

field.

233. The method of claim 232, wherein act (B) comprises:
generating an electric field between at least two electrodes; and
positioning one or more of the semiconductors between the electrodes.

234. The method of claim 231, further comprising an act of:
(B) repeating act (A) with another solution comprising one or more other semiconductors, wherein at least one of the other semiconductor is at least one of the following: a single crystal, an elongated and bulk-doped semiconductor that, at any point along its longitudinal axis, has a largest cross-sectional dimension less than 500 nanometers, and a free-standing and bulk-doped semiconductor with at least one portion having a smallest width of less than 500 nanometers.

235. The method of claim 228, further comprising an act of:
(B) conditioning the surface to attach the one or more contacted semiconductors to the surface.

236. The method of claim 235, wherein act (B) comprises:
forming channels on the surface.

237. The method of claim 235, wherein act (B) comprises:
patterning the surface.

238. The method of claim 228, further comprising:
(B) aligning one or more of the semiconductors on the surface using an electric field.

239. The method of claim 238, wherein act (B) comprises:
generating an electric field between at least two electrodes; and
positioning one or more of the semiconductors between the electrodes.

240. A method of generating light, comprising an act of:

(A) applying energy to one or more semiconductors causing the one or more semiconductors to emit light, wherein at least one of the semiconductors is at least one of the following: a single crystal, an elongated and bulk-doped semiconductor that, at any point along its longitudinal axis, has a largest cross-sectional dimension less than 500 nanometers, and a free-standing and bulk-doped semiconductor with at least one portion having a smallest width of less than 500 nanometers.

241. The method of claim 240, wherein the semiconductor comprises a direct-band-gap semiconductor.

242. The method of claim 240, wherein act (A) comprises applying a voltage across a junction of two crossed semiconductors, each semiconductor having a smallest width of less than 500 nanometers.

243. The method of claim 242, wherein each semiconductor has a smallest width of less than 100 nanometers

244. The method of claim 240, further comprising an act of:

(B) controlling a wavelength of the emitted light by controlling a dimension of the at least one semiconductor having a smallest width of less than 100 nanometers.

245. The method of claim 244, wherein the semiconductor is elongated, and act (B) comprises:

controlling a width of the elongated semiconductor.

246. The method of claim 244, wherein:

the semiconductor has a property that a mass of the semiconductor emits light at a first wavelength if the mass has a minimum shortest dimension, and

the controlled dimension of the semiconductor is less than the minimum shortest dimension.

247. A method of fabricating a device having a doped semiconductor component and one or more other components, the method comprising acts of:

(A) doping a semiconductor during its growth to produce the doped semiconductor component; and

(B) attaching the doped semiconductor component to at least one of the one or more other components.

248. The method of claim 247, wherein the doped semiconductor component is at least one of the following: a single crystal, an elongated and bulk-doped semiconductor that, at any point along its longitudinal axis, has a largest cross-sectional dimension less than 500 nanometers, and a free-standing and bulk-doped semiconductor with at least one portion having a smallest width of less than 500 nanometers.

249.

250. A process for controllably assembling a semiconductor device having elongated elements with a characteristic dimension in a transverse direction of the element on a nanometer scale, comprising:

producing at least one first elements of a first doping type,

orienting said first element in a first direction, and

connecting said first element to at least one first contact to allow an electrical current to flow through the first element.

251. The process of claim 250, further comprising:

producing at least one second element of a second doping type,

orienting said second element in a second direction different from the first direction,

enabling an electrical contact between the first element and the second element, and

connecting said second element to at least one second contact to allow an electrical current to flow between the first and second element.

252. The process of claim 251, wherein the second doping type is n-type if the first doping type is p-type, and p-type if the first doping type is n-type.

253. The process of claim 251, wherein the second element is oriented by applying at least one of an electric field or a fluid flow.

254. The process of claim 250, further comprising:

connecting said first element to spaced-apart contacts and arranging a gate electrode proximate to the first element between the spaced-apart contacts, thereby forming an FET.

255. The process of claim 250, wherein the semiconductor device is made of a material selected from the group consisting of Si, Ge, Sn, Se, Te, B, Diamond, P, B-C, B-P(BP6), B-Si, Si-C, Si-Ge, Si-Sn and Ge-Sn, SiC, BN/BP/BAs, AlN/AlP/AlAs/AlSb, GaN/GaP/GaAs/GaSb, InN/InP/InAs/InSb, BN/BP/BAs, AlN/AlP/AlAs/AlSb, GaN/GaP/GaAs/GaSb, InN/InP/InAs/InSb, ZnO/ZnS/ZnSe/ZnTe, CdS/CdSe/CdTe, HgS/HgSe/HgTe, BeS/BeSe/BeTe/MgS/MgSe, GeS, GeSe, GeTe, SnS, SnSe, SnTe, PbO, PbS, PbSe, PbTe, CuF, CuCl, CuBr, CuI, AgF, AgCl, AgBr, AgI, BeSiN2, CaCN2, ZnGeP2, CdSnAs2, ZnSnSb2, CuGeP3, CuSi2P3, (Cu, Ag)(Al, Ga, In, Tl, Fe)(S, Se, Te)2, Si3N4, Ge3N4, Al2O3, (Al, Ga, In)2(S, Se, Te)3, and Al2CO.

256. The process of claim 250, wherein the first doping type is one of n-type or p-type.

257. The process of claim 250, wherein the first element is oriented by applying at least one of an electric field or a fluid flow.

258. The process of claim 257, wherein the first element is suspended in the fluid flow.

259. The process of claim 250, wherein the first element is oriented by applying a mechanical tool.

260. The process of claim 250, wherein the second element is suspended in the fluid flow.

261. The process of claim 250, wherein the second element is oriented by applying a mechanical tool.

262. A semiconductor device, comprising

a silicon substrate having an array of metal contacts

a crossbar switch element formed in electrical communication with the array and having a first bar formed of a p-type semiconductor nanowire, and

a second bar formed of an n-type semiconductor nanowire and being spaced away from the first bar and being disposed transversely thereto.

263. A semi device of claim 262, wherein the second bar is spaces between 1-10 nm from the first bar.

264. A method for manufacturing a nanowire semiconductor device comprising positioning a first nanowire between two contact points by applying a potential between the contact points; positioning a second nanowire between two other contact points.

265. A method for manufacturing a nanowire semiconductor device comprising forming a surface with one or more regions that selectively attract nanowires.

266. A method for manufacturing a light-emitting diode from nanowires, the diode having an emission wavelength determined by a dimension of a p-n junction between two doped nanowires.

267. A method for manufacturing a semiconductor junction by crossing a p-type nanowire and an n-type nanowire.

268. A method of assembling one or more elongated structures on a surface, the method comprising acts of:

(A) flowing a fluid that comprises the one or more elongated structures onto the surface; and

(B) aligning the one or more elongated structures on the surface to form an array of the elongated structures.

269. The method of claim 268, wherein act (A) comprises flowing the fluid in a first direction and act (B) comprises aligning the one or more elongated structures as the fluid

flows in the first direction to form a first layer of arrayed structures, and wherein the method further comprises:

(C) changing a direction of the flow from the first direction to a second direction; and

(D) repeating acts (A) and (B) in the second direction to form a second layer of arrayed structures.

270. The method of claim 269, comprising repeating acts (C)and (D) one or more times.

271. The method of claim 269, wherein at least a first elongated structure from the first layer contacts at least a second elongated structure from the second array.

272. The method of claim 271, wherein one of the first and second elongated structures is doped semiconductor of a first conductivity type and another of first and second elongated structures is doped semiconductor of a second conductivity type.

273. The method of claim 272, wherein the first conductivity type is p-type and the second conductivity type is n-type, and wherein the first and second elongated structures form a p-n junction.

274. The method of claim 268; wherein the surface is a surface of a substrate.

275. The method of claim 274, wherein the method further comprises:

(C) transferring the array of elongated structures from the surface of the substrate to a surface of another substrate.

276. The method of claim 275, wherein act (C) comprises stamping.

277. The method of claim 268, wherein the one or more elongated structured are aligned onto the surface while still comprised in the fluid.

278. The method of claim 268, wherein the method further comprises:

(C) conditioning the surface with one or more functionalities that attract the one or

more elongated structures to particular positions on the surface,

wherein act (B) comprises attracting the one or more elongated structures to the particular positions using the one or more functionalities.

279. The method of claim 278, wherein act (C) comprises:

conditioning the surface with one or more molecules..

280. The method of claim 278, wherein act (C) comprises:

conditioning the surface with one or more charges.

281. The method of claim 278, wherein act (C) comprises:

conditioning the surface with one or more magnetos.

282. The method of claim 278, wherein act (C) comprises:

conditioning the surface with one or more light intensities.

283. The method of claim 278, wherein act (C) comprises:

conditioning the surface with one or more functionalities that attract the one or more elongated structures to particular positions on the surface using chemical force.

284. The method of claim 278, wherein act (C) comprises:

conditioning the surface with one or more functionalities that attract the one or more elongated structures to particular positions on the surface using optical force.

285. The method of claim 278, wherein act (C) comprises:

conditioning the surface with one or more functionalities that attract the one or more elongated structures to particular positions on the surface using electrostatic force.

286. The method of claim 278, wherein act (C) comprises:

conditioning the surface with one or more functionalities that attract the one or more elongated structures to particular positions on the surface using magnetic force.

287. The method of claim 268, wherein the method further comprises:

(C) patterning the surface to receive the one or more elongated structures at particular positions on the surface.

288. The method of claim 287, wherein act (C) comprises:

creating physical patterns on the surface.

289. The method of claim 288, wherein the physical patterns are trenches.

290. The method of claim 288, wherein the physical patterns are steps.

291. The method of claim 288, wherein the surface is a surface of a substrate, and wherein creating physical patterns on the surface comprises:

using crystal lattice steps of the substrate.

292. The method of claim 288, wherein the surface is a surface of a substrate, and wherein creating physical patterns on the surface comprises:

using self-assembled di-block polymer strips.

293. The method of claim 288, wherein creating physical patterns on the surface comprises:

using patterns.

294. The method of claim 293, wherein creating physical patterns on the surface comprises:

using imprinted patterns.

295. The method of claim 268, wherein act (A) comprises controlling the flow of the fluid using a channel.

296. The method of claim 268, wherein at least one of the elongated structures are semiconductors.

297. The method of claim 268, wherein at least one of the elongated structures are doped semiconductors.

298. The method of claim 297, wherein at least one of the elongated structures are bulk-doped semiconductors.

299. The method of claim 268, wherein at least one of the structures is a doped single-crystal semiconductor.

300. The method of claim 268, wherein at least one of the structures is an elongated and bulk-doped semiconductor that, at any point along its longitudinal axis, has a largest cross-sectional dimension less than 500 nanometers.

301. The method of claim 268, wherein at least one of the structures is a free-standing and bulk-doped semiconductor with at least one portion having a smallest width of less than 500 nanometers.

302. The method of claim 268, wherein at least one of the structures is a doped semiconductor that is at least one of the following: a single crystal, an elongated and bulk-doped semiconductor that, at any point along its longitudinal axis, has a largest cross-sectional dimension less than 500 nanometers, and a free-standing and bulk-doped semiconductor with at least one portion having a smallest width of less than 500 nanometers.

303. The method of claim 302, wherein the doped semiconductor comprises a semiconductor selected from a group consisting of: Si, Ge, Sn, Se, Te, B, Diamond, P, B-C, B-P(BP6), B-Si, Si-C, Si-Ge, Si-Sn and Ge-Sn, SiC, BN/BP/BAs, AlN/AlP/AlAs/AlSb, GaN/GaP/GaAs/GaSb, InN/InP/InAs/InSb, BN/BP/BAs, AlN/AlP/AlAs/AlSb, GaN/GaP/GaAs/GaSb, InN/InP/InAs/InSb, ZnO/ZnS/ZnSe/ZnTe, CdS/CdSe/CdTe, HgS/HgSe/HgTe, BeS/BeSe/BeTe/MgS/MgSe, GeS, GeSe, GeTe, SnS, SnSe, SnTe, PbO, PbS, PbSe, PbTe, CuF, CuCl, CuBr, CuI, AgF, AgCl, AgBr, AgI, BeSiN2, CaCN2, ZnGeP2, CdSnAs2, ZnSnSb2, CuGeP3, CuSi2P3, (Cu, Ag)(Al, Ga, In, Tl, Fe)(S, Se,

Te)2, Si3N4, Ge3N4, Al2O3, (Al, Ga, In)2(S, Se, Te)3, Al2CO.

304. The method of claim 302, wherein the doped semiconductor comprises a dopant selected from a group consisting of:: a p-type dopant from Group III of the periodic table; an n-type dopant from Group V of the periodic table; a p-type dopant selected from a group consisting of: B, Al and In; an n-type dopant selected from a group consisting of: P, As and Sb; a p-type dopant from Group II of the periodic table; a p-type dopant selected from a group consisting of: Mg, Zn, Cd and Hg; a p-type dopant from Group IV of the periodic table; a p-type dopant selected from a group consisting of: C and Si.; and an n-type is selected from a group consisting of: Si, Ge, Sn, S, Se and Te.

305. The method of claim 302, wherein the doped semiconductor is doped during growth of the semiconductor.

306. A method of assembling one or more elongated structures on a surface, wherein one or more of the elongated structures are at least one of the following: a single crystal, an elongated and bulk-doped semiconductor that, at any point along its longitudinal axis, has a largest cross-sectional dimension less than 500 nanometers, and a free-standing and bulk-doped semiconductor with at least one portion having a smallest width of less than 500 nanometers, and wherein the method comprises acts of:

(A) conditioning the surface with one or more functionalities that attract the one or more elongated structures to particular positions on the surface, and

(B) aligning the one or more elongated structures by attracting the one or more elongated structures to the particular positions using the one or more functionalities.

307. The method of claim 306, wherein act (A) comprises:
conditioning the surface with one or more molecules..

308. The method of claim 306, wherein act (A) comprises:
conditioning the surface with one or more charges.

309. The method of claim 306, wherein act (A) comprises:

conditioning the surface with one or more magnetos.

310. The method of claim 306, wherein act (A) comprises:

conditioning the surface with one or more light intensities.

311. The method of claim 306, wherein act (A) comprises:

conditioning the surface with one or more functionalities that attract the one or more elongated structures to particular positions on the surface using chemical force.

312. The method of claim 306, wherein act (A) comprises:

conditioning the surface with one or more functionalities that attract the one or more elongated structures to particular positions on the surface using optical force.

313. The method of claim 306, wherein act (A) comprises:

conditioning the surface with one or more functionalities that attract the one or more elongated structures to particular positions on the surface using electrostatic force.

314. The method of claim 306, wherein act (A) comprises:

conditioning the surface with one or more functionalities that attract the one or more elongated structures to particular positions on the surface using magnetic force.

315. A method of assembling a plurality of elongated structures on a surface, wherein one or more of the elongated structures are at least one of the following: a single crystal, an elongated and bulk-doped semiconductor that, at any point along its longitudinal axis, has a largest cross-sectional dimension less than 500 nanometers, and a free-standing and bulk-doped semiconductor with at least one portion having a smallest width of less than 500 nanometers, and wherein the method comprises acts of:

(A) depositing the plurality of elongated structures onto the surface; and

(B) electrically charging the surface to produce electrostatic forces between two or more of the plurality of the elongated structures.

316. The method of claim 315, wherein the electrostatic forces cause the two or more elongated structures to align themselves.

317. The method of claim 316, wherein the electrostatic forces cause the two or more elongated structures to align themselves into one or more patterns.

318. The method of claim 317, wherein the one or more patterns comprise a parallel array.

319. A method of assembling a plurality of elongated structures on a surface, wherein one or more of the elongated structures are at least one of the following: a single crystal, an elongated and bulk-doped semiconductor that, at any point along its longitudinal axis, has a largest cross-sectional dimension less than 500 nanometers, and a free-standing and bulk-doped semiconductor with at least one portion having a smallest width of less than 500 nanometers, and wherein the method comprises acts of:

(A) dispersing the one or more elongated structures on a surface of a liquid phase to form a Langmuir-Blodgett film;

(B) compressing the Langmuir-Blodgett film; and

(C) transferring the compressed Langmuir-Blodgett film onto a surface

320. The method of claim 319, wherein the surface id the surface of a substrate.

321. A method of assembling a plurality of one or more elongated structures on a surface, wherein at least one of the elongated structures are at least one of the following: a single crystal, an elongated and bulk-doped semiconductor that, at any point along its longitudinal axis, has a largest cross-sectional dimension less than 500 nanometers, and a free-standing and bulk-doped semiconductor with at least one portion having a smallest width of less than 500 nanometers, and wherein the method comprises acts of:

(A) dispersing the one or more elongated structures in a flexible matrix;

(B) stretching the flexible matrix in a direction to produce a shear force on the one or more elongated structures that causes the at least one elongated structure to align in the direction;

(C) removing the flexible matrix; and

(D) transferring the at least one aligned elongated structure to a surface.

322. The method of claim 321, wherein the direction is parallel to a plane of the surface.

323. The method of claim 321, wherein act (B) comprises:
stretching the flexible matrix with an electrically-induced force.

324. The method of claim 321, wherein act (B) comprises:
stretching the flexible matrix with an optically-induced force.

325. The method of claim 321, wherein act (B) comprises:
stretching the flexible matrix with a mechanically-induced force.

326. The method of claim 321, wherein act (B) comprises:
stretching the flexible matrix with a magnetically-induced force.

327. The method of claim 321, wherein the surface is a surface of a substrate.

328. The method of claim 321, wherein the flexible matrix is a polymer.

329. A system for growing a doped semiconductor, the system comprising:
means for providing a molecules of the semiconductor and molecules of a dopant; and
means for doping the molecules of the semiconductor with the molecules of the dopant during growth of the semiconductor to produce the doped semiconductor.

330. A system for assembling one or more elongated structures on a surface, the system comprising:
means for flowing a fluid that comprises the one or more elongated structures onto the surface; and
means for aligning the one or more elongated structures on the surface to form an array of the elongated structures.

331. A system for assembling one or more elongated structures on a surface, wherein one or more of the elongated structures are at least one of the following: is at least one of the following: a single crystal, an elongated and bulk-doped semiconductor that, at any point along its longitudinal axis, has a largest cross-sectional dimension less than 500 nanometers, and a free-standing and bulk-doped semiconductor with at least one portion having a smallest width of less than 500 nanometers, and wherein the system comprises:

means for conditioning the surface with one or more functionalities that attract the one or more elongated structures to particular positions on the surface, and

means for aligning the one or more elongated structures by attracting the one or more elongated structures to the particular positions using the one or more functionalities.

332. A system for assembling a plurality of elongated structures on a surface, wherein one or more of the elongated structures are at least one of the following: is at least one of the following: a single crystal, an elongated and bulk-doped semiconductor that, at any point along its longitudinal axis, has a largest cross-sectional dimension less than 500 nanometers, and a free-standing and bulk-doped semiconductor with at least one portion having a smallest width of less than 500 nanometers, and wherein the system comprises

means for depositing the plurality of elongated structures onto the surface; and

means for electrically charging the surface to produce electrostatic forces between two or more of the plurality of the elongated structures.

333. A system for assembling a plurality of elongated structures on a surface, wherein one or more of the elongated structures are at least one of the following: is at least one of the following: a single crystal, an elongated and bulk-doped semiconductor that, at any point along its longitudinal axis, has a largest cross-sectional dimension less than 500 nanometers, and a free-standing and bulk-doped semiconductor with at least one portion having a smallest width of less than 500 nanometers, and wherein the system comprises:

means for dispersing the one or more elongated structures on a surface of a liquid phase to form a Langmuir-Blodgett film;

means for compressing the Langmuir-Blodgett film; and

means for transferring the compressed Langmuir-Blodgett film onto a surface

334. A system for assembling a plurality of one or more elongated structures on a surface, wherein at least one of the elongated structures are at least one of the following: a single crystal, an elongated and bulk-doped semiconductor that, at any point along its longitudinal axis, has a largest cross-sectional dimension less than 500 nanometers, and a free-standing and bulk-doped semiconductor with at least one portion having a smallest width of less than 500 nanometers, and wherein the system comprises:

means for dispersing the one or more elongated structures in a flexible matrix;

means for stretching the flexible matrix in a direction to produce a shear force on the one or more elongated structures that causes the at least one elongated structure to align in the direction;

means for removing the flexible matrix; and

means for transferring the at least one aligned elongated structure to a surface.